Abstracts

A 2 Gb/s Throughput GaAs Digital Time Switch LSI Using LSCFL (Dec. 1985 [T-MTT])

T. Takada, Y. Shimazu, K. Yamasaki, M. Togashi, K. Hoshikawa and M. Idda. "A 2 Gb/s Throughput GaAs Digital Time Switch LSI Using LSCFL (Dec. 1985 [T-MTT])." 1985 Transactions on Microwave Theory and Techniques 33.12 (Dec. 1985 [T-MTT] (1985 Symposium Issue)): 1579-1584.

A GaAs four-channel digital time switch LSI with a 2.0-Gb/s throughput is developed. This switch consists of 4-bit shift registers, data latches, a counter, a control unit, and 1/0 buffer gates. The LSI includes 1176 devices (FET's, diodes, and resistors) and its equivalent gate number is 231 gates. Low Power Source Coupled FET Logic (LSCFL) operating in a true/complementary mode is used to ensure high-speed and low-power performance. MESFET's with 0.55-µm gate length are fabricated by the buried p-layer SAINT process, which satisfactorily suppresses short channel effects. Dislocation-free wafers are also used to provide high chip yields of 75 percent. The propagation delay time of the LSCFL basic circuit is 48 ps/gate with 1.4-mW/equivalent gate. The total power dissipation including input and output buffers is 0.64 W. The LSI speed performance is evaluated by measuring toggle frequency of the 1/4 frequency divider. The divider operates typically at 5.1 GHz, maximum 7.5 GHz. The newly developed high-speed digital time switch LSI makes possible time division switching services in TV and high-definition TV transmission systems.

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